AMENDMENTS TO THE CLAIMS

Claims 1-9. (Cancelled).

10. (Currently Amended) A method of manufacturing a semiconductor device, the method comprising:

forming a gate electrode, having side surfaces, over an upper surface of a substrate with a gate dielectric layer therebetween;

~~forming a composite liner comprising:~~

depositing an oxide liner, by decoupled plasma deposition at a temperature no greater than about 400° C, on the side surface of the gate electrode and the upper surface of the substrate; ~~and~~

depositing a nitride liner on the oxide liner by decoupled plasma deposition at a temperature no greater than about 400°C; and

forming a sidewall spacer on the nitride ~~composite~~ liner.

11. (Original) The method according to claim 10, wherein:

the oxide liner comprises a silicon oxide;

the nitride liner comprises a silicon nitride; and

the sidewall spacer comprises a silicon oxide, silicon nitride or silicon oxynitride.

12. (Original) The method according to claim 11, comprising forming the sidewall spacer of a silicon oxide having a dielectric constant (k) no greater than about 3.9.

Claims 13-15. (Cancelled).

16. (Currently Amended) The method according to claim 11, comprising ion implanting to form shallow source/drain extensions in the upper surface of the substrate, using the gate electrode as a mask, before depositing ~~forming~~ the ~~composite~~ oxide liner.

17. (Original) The method according to claim 16, comprising ion implanting a P-type impurity to form the source/drain extension.

18. (Original) The method according to claim 17, wherein the P-type impurity comprises boron.

19. (Original) The method according to claim 18, comprising forming the source/drain extensions at a junction depth (X_j) of about 200 Å to about 300 Å.

20. (New) The method according to claim 10, comprising:

depositing the silicon oxide liner at a thickness of about 10 Å to about 50 Å; and

depositing the silicon nitride liner at a thickness of about 50 Å to about 200 Å.